

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE****C. Amendments to the Claims.**

1. (Previously Amended) An integrated circuit device, comprising:

5 a programmable portion comprising a plurality of circuits  
configurable by a user of the integrated circuit device; and

at least one communication portion comprising at least one circuit  
block manufactured to perform a predetermined data communication  
function including converting received first data values into second data  
values.

10 2. (Original) The integrated circuit device of claim 1, wherein:

the programmable portion comprises a programmable interconnect  
portion and a logic gate portion.

15 3. (Original) The integrated circuit device of claim 2, further including:

a memory circuit for storing configuration information for  
configuring circuits of the programmable portion.

4. (Original) The integrated circuit device of claim 2, further including:

20 a timing circuit that receives a clock signal and generates an  
internal clock signal that is phase shifted with respect to the clock signal.

5. (Original) The integrated circuit device of claim 1, further including:

25 a plurality of input/outputs commonly connected to the  
programmable portion and the communication portion.

6. (Original) The integrated circuit device of claim 1, wherein:

30 the communication portion includes a plurality of data operation  
circuits, each of which performs a different function on received input  
data.

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7. (Currently Amended) The integrated circuit device of claim 6, wherein:

the data operation circuits include a block converter circuit that ~~may~~ converts an input data word into an output data word having different bit values than the input data word.

5 8. (Currently Amended) The integrated circuit device of claim 6, wherein:

the data operation circuits include a scrambler circuit that ~~may~~ performing a scramble operation on the received data ~~that may be~~ represented by a scrambling polynomial.

9. (Original) The integrated circuit device of claim 6, wherein:

10 the communication portion further includes an operation control store that provides one of a plurality of operational values to the data operation circuits that controls the type of operation performed on the received data.

10. (Original) The integrated circuit device of claim 9, wherein:

15 the data operation circuits include a scrambler circuit that may perform a scramble operation on the received data; and  
the operation control store provides operational values that represent at least one scrambling polynomial.

11. (Original) The integrated circuit device of claim 9, wherein:

20 the operational control store includes circuits that may provide at least one user operational value configured by a user and preset operational values that may be established by at least one integrated circuit manufacturing step.

12. (Original) The integrated circuit device of claim 6, wherein:

25 the communication portion includes a data (MUX) multiplexer that enables a data path between one of a plurality of inputs and a data MUX

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output, and each data operation circuit is coupled to an input of the data MUX.

13. (Original) The integrated circuit device of claim 6, wherein:

the communication portion includes a physical layer circuit that provides a data output stream compatible with a particular data transmission media.

14. (Original) The integrated circuit device of claim 6, wherein:

the at least one communication portion includes a plurality of communication portions.

15. (Original) A semiconductor device, comprising:

a programmable logic device having a communication portion embedded therein, the communication portion including non-programmable circuits designed to provide a selectable data communication function.

16. (Original) The semiconductor device of claim 15, wherein:

the communication portion includes a plurality of circuit blocks that each provides a different data communication function.

17. (Original) The semiconductor device of claim 16, wherein:

the communication portion includes a selectable data path between each circuit block and a data output.

18. (Original) The semiconductor device of claim 15, wherein:

the communication portion includes a block converter circuit that encodes input data words into output data words and a scrambler circuit that scrambles data values according to an operational control value.

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19. (Original) The semiconductor device of claim 15, wherein:

the communication portion includes a block converter circuit that decodes input data words into output data words and a de-scrambler circuit that de-scrambles data values according to an operational control value.

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20. (Original) The semiconductor device of claim 18, wherein:

the communication portion includes an operational control store that provides selectable operational control values to the scrambler circuit.

21. (Currently Amended) A method, comprising the steps of:

performing predetermined logic functions on a programmable logic portion of ~~the an~~ integrated circuit; and

performing serial data communication functions on a communication portion of the integrated circuit that includes circuit blocks that are not synthesized with programmable logic device configuration data.

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22. (Original) The method of claim 21, wherein:

performing serial data communication functions includes

selecting a polynomial value from a number of polynomial

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values, and

scrambling serial data according to the selected polynomial value.

23. (Original) The method of claim 21, wherein:

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performing serial data communication functions includes encoding serial data having words of a first bit length into serial data having words of a second bit length that is different than the first bit length.

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